



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,191	05/20/2004	Tsukasa Shiraishi	2004-0787	7292

513 7590 07/10/2006

WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER

WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
----------	--------------

2826

DATE MAILED: 07/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/849,191

Applicant(s)

SHIRAISHI ET AL.

Examiner

Alexander O. Williams

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 April 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2826

Serial Number: 10/849191 Attorney's Docket #: 2004_0787

Filing Date: 5/20/2004; claimed foreign priority to 11/29/2000

Applicant: Shiraishi et al.

Examiner: Alexander Williams

Applicant's Amendment filed 4/21/06 to the election without traverse of species figure 6 (claims 1 to 3), filed 5/12/05, has been acknowledged.

Claims 1 to 3 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear and confusing to what is meant by "at least a first semiconductor element mounted on said first side of said multilayer wiring board and a **second semiconductor element mounted said second side of said multilayer wiring board.**" Should this be "a second semiconductor element mounted "on" said first side of said multilayer wiring board? One of the "said" should probably be deleted.

In claim 3, it is unclear and confusing to what is meant by "wherein **said said** semiconductor device and said mother multilayer wiring board are electrically connected by an electrically conductive supporting body."

Any of claims 1 to 3 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 to 3, insofar as they can be understood, are rejected under 35 U.S.C. § 102(b) as being anticipated by Braun (U.S. Patent # 4,882,657).

1. Braun (figures 1 to 3) specifically figure 2 show a semiconductor device module comprising: a semiconductor device including: a multi-layer wiring board 61 having a first side 64 and a second side 66, said multi-layer wiring board including a plurality of insulation layers 62 each having a first side and a second side, and including a plurality of circuit pattern layers 90 arranged such that one of said circuit pattern layers is located on each of said first side and said second side of each of said insulating layers, said insulation layers and said circuit pattern layers being alternatively laminated, and wherein each of said insulation layers has a plurality of inner via holes extending between said first side and said second side of each of said insulation layers and electrically connecting said circuit pattern layers so as to define a three-dimensional wiring pattern; and; at least a first semiconductor element 68,70,72 mounted on said first side of said multi-layer wiring board and a second semiconductor element 74,76,78 mounted said second side of said multi-layer wiring board wherein electrodes of said first semiconductor element and said second semiconductor element are connected with each other by said three-dimensional wiring pattern of said multi-layer wiring board; and a mother multi-layer wiring board 96 having a circuit pattern formed on a surface thereof, wherein said semiconductor device is mounted on said mother multi-layer wiring board and said semiconductor device and said mother multi-layer wiring board are electrically connected.

Art Unit: 2826

2. The semiconductor device module according to claim 1, Braum et al. show wherein said semiconductor device and said mother multi-layer wiring board are electrically connected by a projecting electrode which is interposed between said multi-layer wiring board of said semiconductor device and said mother multi-layer wiring board by bonding said back surface of said second semiconductor element onto said mother multi-layer wiring board thus placing said semiconductor device on said mother multi-layer wiring board, thereby connecting said circuit pattern provided on said multi-layer wiring board and said circuit pattern provided on said mother multi-layer wiring board.

3. The semiconductor device module according to claim 1, Braum show wherein said semiconductor device and said mother multi-layer wiring board are electrically connected by an electrically conductive supporting body which is electrically connected to said three-dimensional wiring pattern of said multi-layer wiring board of said semiconductor device and which also fastens said semiconductor device onto said mother multi-layer wiring board, so as to establish electrical connection between said three-dimensional wiring pattern of said multi-layer wiring board of said semiconductor device and said circuit pattern provided on said mother multi-layer wiring board by fastening said semiconductor device onto said mother multi-layer wiring board via said electrically conductive supporting body.

Claims 1 to 3, insofar as they can be understood, are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu et al. (U.S. Patent # 5,438,224.

1. Wu et al. (figures 1 to 6) specifically figures 3 and 4 show a semiconductor device module comprising: a semiconductor device

Art Unit: 2826

including: a multi-layer wiring board **22,32** having a first side **26** and a second side **36**, said multi-layer wiring board including a plurality of insulation layers each having a first side and a second side, and including a plurality of circuit pattern layers arranged such that one of said circuit pattern layers is located on each of said first side and said second side of each of said insulating layers, said insulation layers and said circuit pattern layers being alternatively laminated, and wherein each of said insulation layers has a plurality of inner via holes extending between said first side and said second side of each of said insulation layers and electrically connecting said circuit pattern layers so as to define a three-dimensional wiring pattern; and; at least a first semiconductor element **24** mounted on said first side of said multi-layer wiring board and a second semiconductor element **34** mounted said second side of said multi-layer wiring board wherein electrodes of said first semiconductor element and said second semiconductor element are connected with each other by said three-dimensional wiring pattern of said multi-layer wiring board; and a mother multi-layer wiring board **15** having a circuit pattern formed on a surface thereof, wherein said semiconductor device is mounted on said mother multi-layer wiring board and said semiconductor device and said mother multi-layer wiring board are electrically connected.

2. The semiconductor device module according to claim 1, Wu et al. show wherein said said semiconductor device and said mother multi-layer wiring board are electrically connected by a projecting electrode which is interposed between said multi-layer wiring board of said semiconductor device and said mother multi-layer wiring board by bonding said back surface of said

Art Unit: 2826

second semiconductor element onto said mother multi-layer wiring board thus placing said semiconductor device on said mother multi-layer wiring board, thereby connecting said circuit pattern provided on said multi-layer wiring board and said circuit pattern provided on said mother multi-layer wiring board.

3. The semiconductor device module according to claim 1, Wu et al. show wherein said semiconductor device and said mother multi-layer wiring board are electrically connected by an electrically conductive supporting body which is electrically connected to said three-dimensional wiring pattern of said multi-layer wiring board of said semiconductor device and which also fastens said semiconductor device onto said mother multi-layer wiring board, so as to establish electrical connection between said three-dimensional wiring pattern of said multi-layer wiring board of said semiconductor device and said circuit pattern provided on said mother multi-layer wiring board by fastening said semiconductor device onto said mother multi-layer wiring board via said electrically conductive supporting body.

Response

Applicant's arguments filed 4/21/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1-3" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION.

Art Unit: 2826

IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

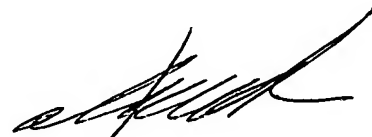
Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,778,734,668,779,700,701,758,691,6 98,E25.013,E23.114,e23.064,e25.011,e23.172 361/767,768,803,818,792,760,763,782,784,794,795	7/21/05 12/29/05 7/5/06
Other Documentation: foreign patents and literature in 257/686,685,723,777,778,734,668,779,700,701,758,691,6 98,E25.013,E23.114,e23.064,e25.011,e23.172 361/767,768,803,818,792,760,763,782,784,794,795	7/21/05 12/29/05 7/5/06
Electronic data base(s): U.S. Patents EAST	7/21/05 12/29/05 7/5/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

Art Unit: 2826

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
7/5/06